ABSTRACT

An integrated circuit, comprising a processor, an onboard system clock for generating a clock signal, and clock trim circuitry, the integrated circuit being configured to: (a) receive an external signal; (b) determine either the number of cycles of the clock signal during a predetermined number of cycles of the external signal, or the number of cycles of the external signal during a predetermined number of cycles of the clock signal; (c) store a trim value in the integrated circuit, the trim value having been determined on the basis of the determined number of cycles; and (d) use the trim value to control the internal clock frequency.